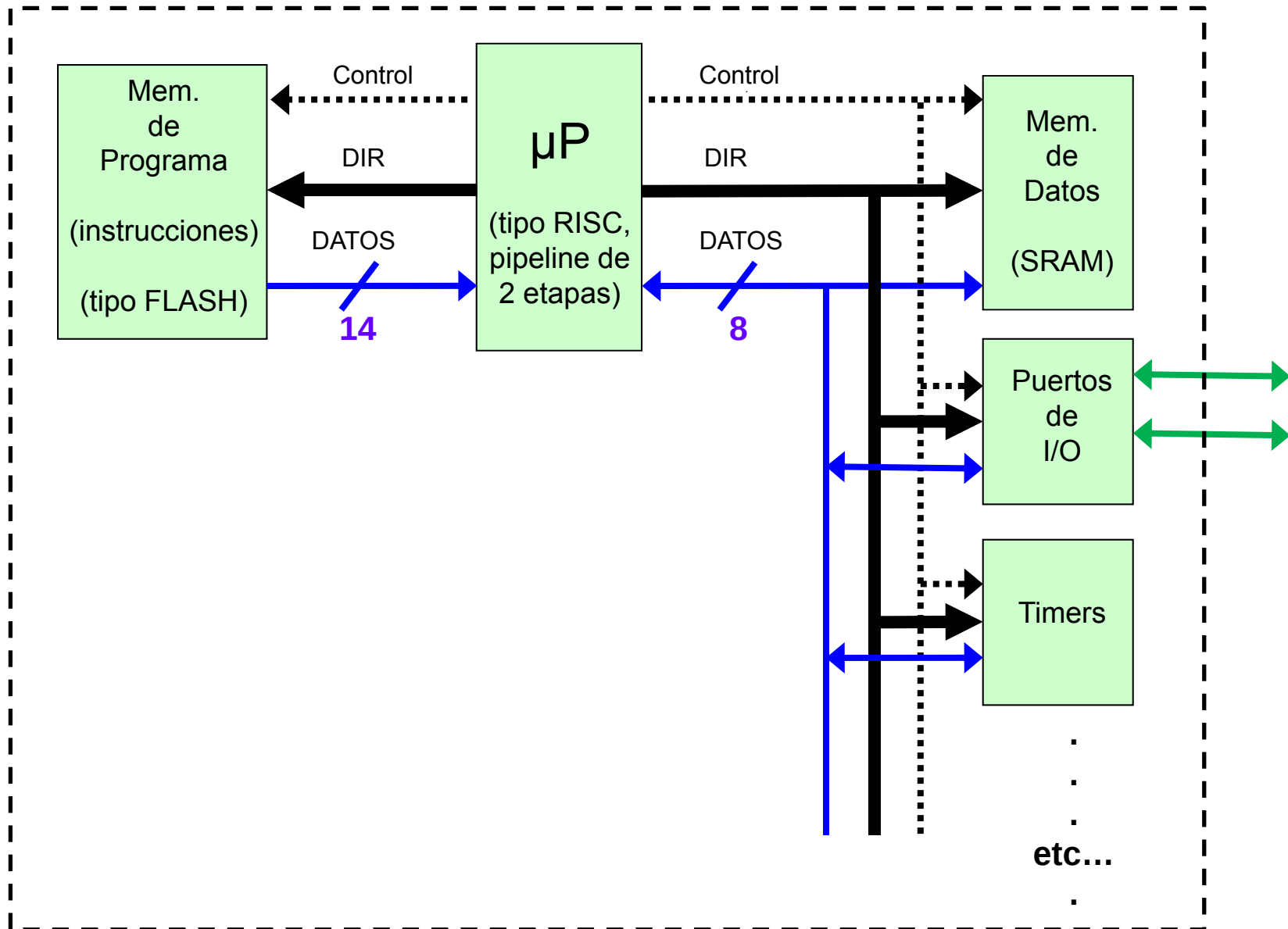


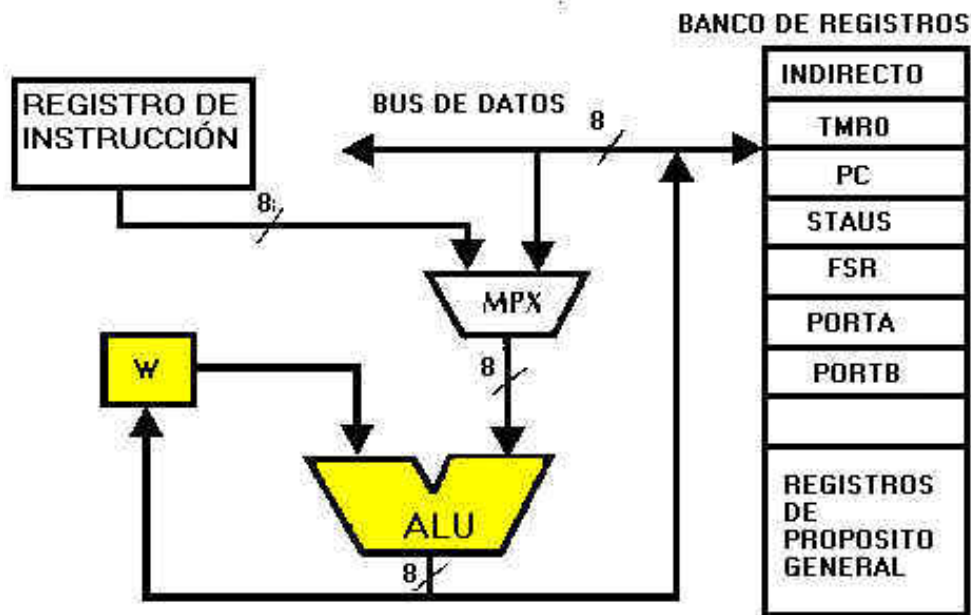
Microcontrolador PIC16F84: Arquitectura

La arquitectura del PIC es tipo Harvard:



Microcontrolador PIC16F84: características básicas

Esquema simplificado del uP de un PIC:



Archivo de registros:

- Se organiza en bancos (PIC16F84: 2 bancos).
- From 00h to 0Bh: special function registers (SFR).
- From 0Ch to 4Fh: general purpose registers (GPR).

SFR
(15)

GPR
(68)

File Address		File Address	
00h	Indirect addr. ⁽¹⁾	Indirect addr. ⁽¹⁾	80h
01h	TMR0	OPTION_REG	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	—	—	87h
08h	EEDATA	EECON1	88h
09h	EEADR	EECON2 ⁽¹⁾	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	68 General Purpose Registers (SRAM) Mapped (accesses) in Bank 0		8Ch
4Fh			
50h			D0h
7Fh			FFh
Bank 0		Bank 1	

Unimplemented data memory location, read as '0'.

Note 1: Not a physical register.

Microcontrolador PIC16F84: características básicas

Características del registro PC:

- Es de 13 bits $\rightarrow 2^{13} = 8K$ máximo de memoria de programa.

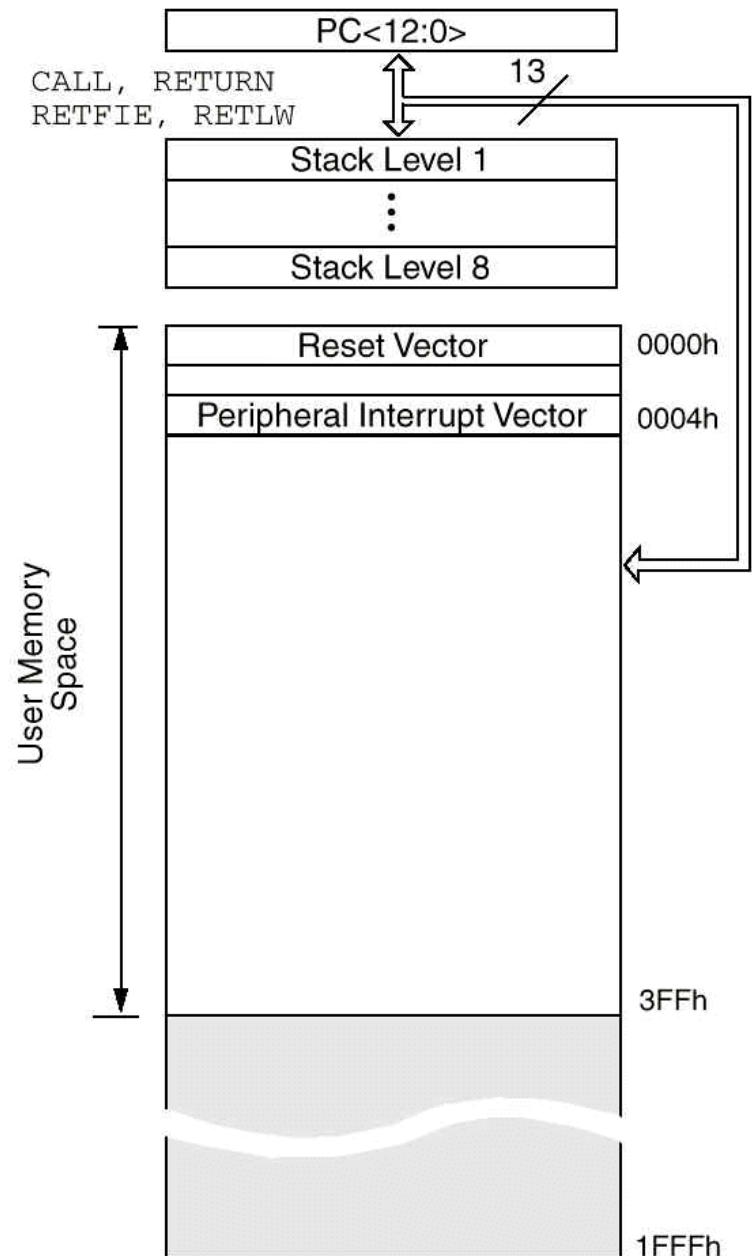
- Se distinguen los siguientes registros:

PCL: Byte menos significativo de PC<7...0>. Accesible al usuario de forma directa para lectura y escritura). Escribir en **PCL** implica hacer un salto (llamado salto programado).

PCH: parte alta de PC <12...8>. No es accesible directamente por el usuario.

PCLATH: **PCH** se puede modificar escribiendo en este registro que es accesible por el usuario solo para escritura. No se ve modificado por las instrucciones CALL y GOTO (que contienen una dirección de solo 11 bits).

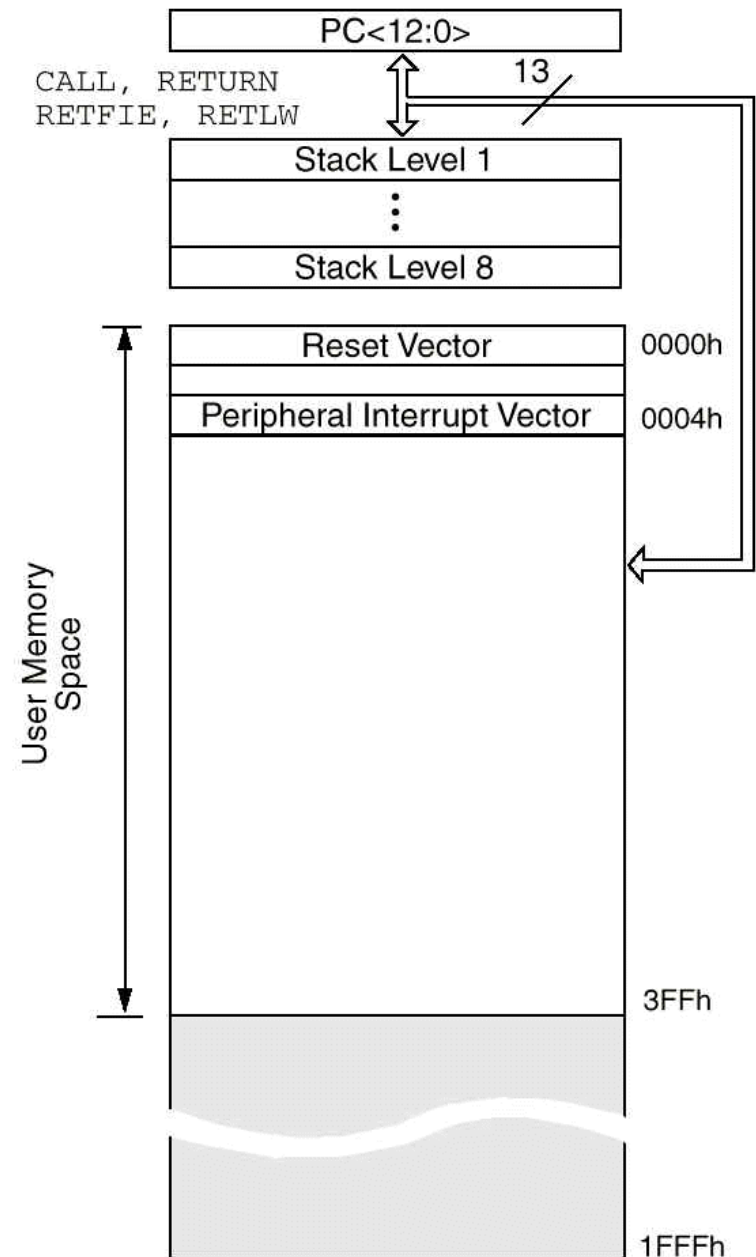
- Rango del “salto programado”: 256 instrucciones.
- Rango del CALL o GOTO: 2048 (2K) instrucciones.



Microcontrolador PIC16F84: características básicas

Características de la pila (o stack):

- No está implementada en RAM (como en el 8085) sino que tiene su propia memoria en el “interior” del μ P del PIC.
- Sólo se utiliza para las llamadas y retornos de subrutinas: CALL e interrupciones.
- No existen las instrucciones PUSH y POP.
- La recuperación de la pila (retorno) se realiza exclusivamente a través de las instrucciones tipo RET: RETURN, RETLW y RETFIE.
- Tiene un ancho de 13 bits (no hay que tener en cuenta la diferenciación PCL-PCH-PCLATCH).
- La pila solo tiene 8 niveles. Almacenar un noveno dato implica sustituir el primer dato almacenado por el nuevo.



Microcontrolador PIC16F84: Registros de funciones especiales (SFR)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on RESET	Details on page
Bank 0											
00h	INDF	Uses contents of FSR to address Data Memory (not a physical register)								---- --	11
01h	TMR0	8-bit Real-Time Clock/Counter								xxxx xxxx	20
02h	PCL	Low Order 8 bits of the Program Counter (PC)								0000 0000	11
03h	STATUS ⁽²⁾	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	8
04h	FSR	Indirect Data Memory Address Pointer 0								xxxx xxxx	11
05h	PORTA ⁽⁴⁾	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	16
06h	PORTB ⁽⁵⁾	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	18
07h	—	Unimplemented location, read as '0'								—	—
08h	EEDATA	EEPROM Data Register								xxxx xxxx	13,14
09h	EEADR	EEPROM Address Register								xxxx xxxx	13,14
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of the PC ⁽¹⁾				---0 0000	11	
0Bh	INTCON	GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	10
Bank 1											
80h	INDF	Uses Contents of FSR to address Data Memory (not a physical register)								---- --	11
81h	OPTION_REG	RBPV	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	9
82h	PCL	Low order 8 bits of Program Counter (PC)								0000 0000	11
83h	STATUS ⁽²⁾	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	8
84h	FSR	Indirect data memory address pointer 0								xxxx xxxx	11
85h	TRISA	—	—	—	PORTA Data Direction Register				---1 1111	16	
86h	TRISB	PORTB Data Direction Register								1111 1111	18
87h	—	Unimplemented location, read as '0'								—	—
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	13
89h	EECON2	EEPROM Control Register 2 (not a physical register)								---- --	14
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC ⁽¹⁾				---0 0000	11	
0Bh	INTCON	GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	10

Legend: x = unknown, u = unchanged. - = unimplemented, read as '0', q = value depends on condition

Microcontrolador PIC16F84: Status

REGISTER 2-1: STATUS REGISTER (ADDRESS 03h, 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C
bit 7			bit 0				

- bit 7-6 **Unimplemented:** Maintain as '0'
- bit 5 **RP0:** Register Bank Select bits (used for direct addressing)
 01 = Bank 1 (80h - FFh)
 00 = Bank 0 (00h - 7Fh)
- bit 4 **$\overline{\text{TO}}$:** Time-out bit
 1 = After power-up, CLRWDT instruction, or SLEEP instruction
 0 = A WDT time-out occurred
- bit 3 **$\overline{\text{PD}}$:** Power-down bit
 1 = After power-up or by the CLRWDT instruction
 0 = By execution of the SLEEP instruction
- bit 2 **Z:** Zero bit
 1 = The result of an arithmetic or logic operation is zero
 0 = The result of an arithmetic or logic operation is not zero
- bit 1 **DC:** Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) (for borrow, the polarity is reversed)
 1 = A carry-out from the 4th low order bit of the result occurred
 0 = No carry-out from the 4th low order bit of the result
- bit 0 **C:** Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) (for borrow, the polarity is reversed)
 1 = A carry-out from the Most Significant bit of the result occurred
 0 = No carry-out from the Most Significant bit of the result occurred
- Note:** A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

Microcontrolador PIC16F84: Set de instrucciones

TABLE 9-2 PIC16FXX INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	14-Bit Opcode				Status Affected	Notes	
			MSb		LSb				
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	2
CLRWF	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECf	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDt	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	TO,PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

f: indica alguno de los registros (SFR ó GPR).

d: indica el destino de la operación (0: W; 1: f)

b: indica el bit (=0...7).

k: dato literal (8-bits).

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

Algunas equivalencias de terminología (entre 8085 y PIC)

8085

PIC

Reg. "A" (acumulador) → Reg. "W" (working register)

"Registros" (B,C,D,E,PC, etc.) → "Files" (SFRs, GPRs)

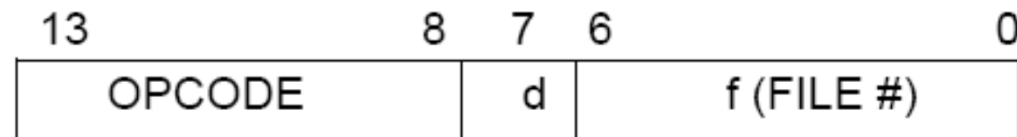
Direccionamiento inmediato → Direccionamiento literal
Ej. MVI, ADI, etc Ej. MOVLW, ADDLW, etc

Direccionamiento a registro → Direccionamiento directo
Ej. MOV A,E Ej. MOVWF 03h

Microcontrolador PIC16F84: Instruction word

Instrucciones con direccionamiento directo:

Byte-oriented file register operations

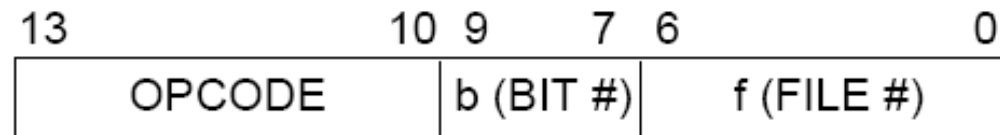


d = 0 for destination W

d = 1 for destination f

f = 7-bit file register address

Bit-oriented file register operations



b = 3-bit bit address

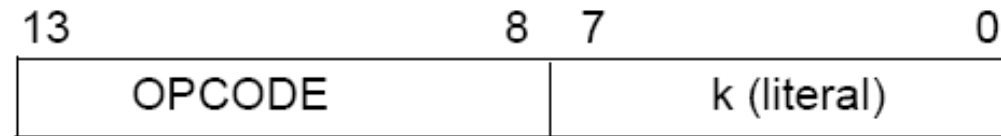
f = 7-bit file register address

Microcontrolador PIC16F84: Instruction word

Instrucciones con direccionamiento inmediato o literal:

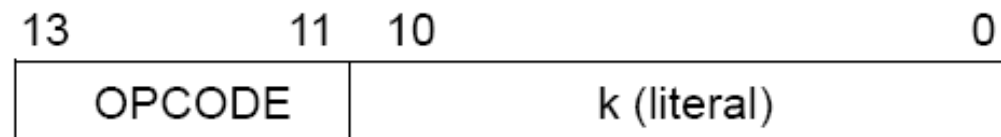
Literal and control operations

General



k = 8-bit immediate value

CALL and GOTO instructions only



k = 11-bit immediate value

Microcontroladores PIC: Assembler

Particularidades del assembler para PIC:

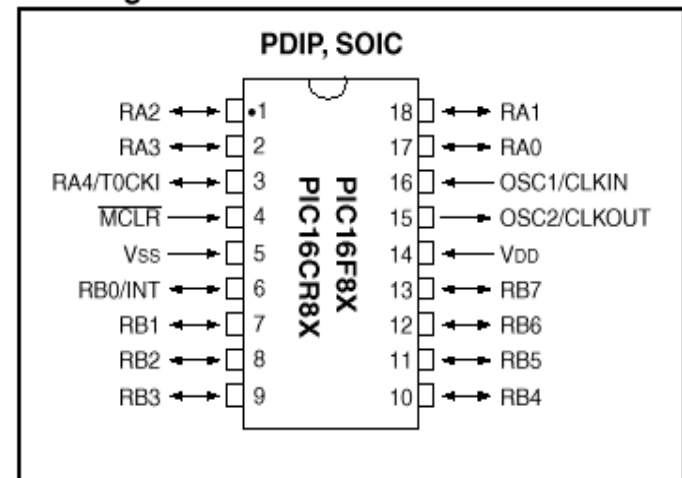
- Emplea los mnemotécnicos de las instrucciones del μ C al cual está dirigido. En nuestro caso corresponderá al set de instrucciones de los PICs de la gama media (solo 35 instrucciones).
- Permite la utilización de etiquetas, tanto para apuntar a direcciones como para definir valores constantes.
- Es posible expresar las cantidades numéricas en diferentes bases, siendo la base por defecto la hexadecimal.
- Existen una serie de pseudo-instrucciones o directivas (además de las ya conocidas ORG, EQU y END) específicas para estos μ Cs.
- Se guarda en un archivo en formato ASCII, utilizando la extensión *.ASM

Microcontrolador PIC16F84: Puertos de I/O

Puertos de entrada / salida:

- Se dispone de un total de 13 líneas, programables individualmente como entrada o salida.
- Se distribuyen en dos puertos: PORTA y PORTB.
- Se accede a cada puerto leyendo o escribiendo en los registros (files) 05h y 06h (Bank 0).
- La configuración de cada línea como entrada o salida la determinan los bits de los registros TRISA y TRISB en las posiciones 85h y 86h (05h y 06h del Bank 1), según:
 - '1' línea configurada como entrada.
 - '0' línea configurada como salida.

Pin Diagrams



Microcontrolador PIC16F84: Puertos de I/O

Configuración y acceso a los puertos:

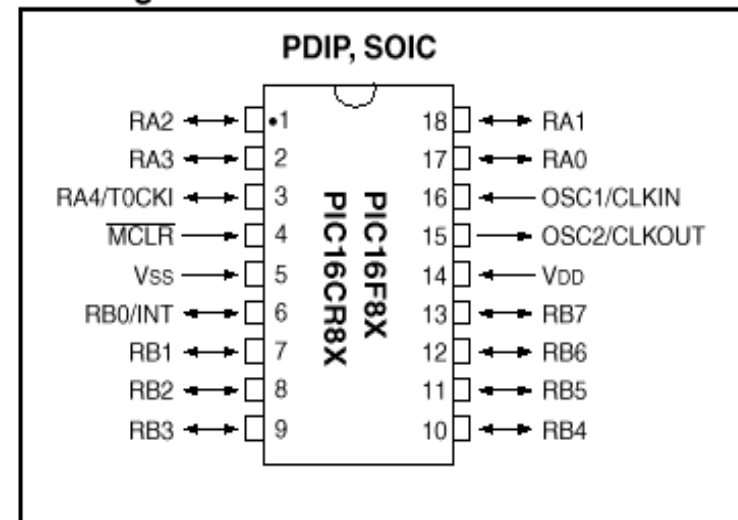
Bank 0:

05h	PORTA ⁽⁴⁾	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	16
06h	PORTB ⁽⁵⁾	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	18

Bank 1:

85h	TRISA	—	—	—	PORTA Data Direction Register	---1 1111	16
86h	TRISB	PORTB Data Direction Register				1111 1111	18

Pin Diagrams



Microcontrolador PIC16F84: Oscilador del Clock

Cuatro modos de funcionamiento:

- LP: Low Power Crystal
- XT: Crystal/Resonator
- HS: High Speed Crystal/Resonator
- RC: Resistencia/Condensador

FIGURE 8-3: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)

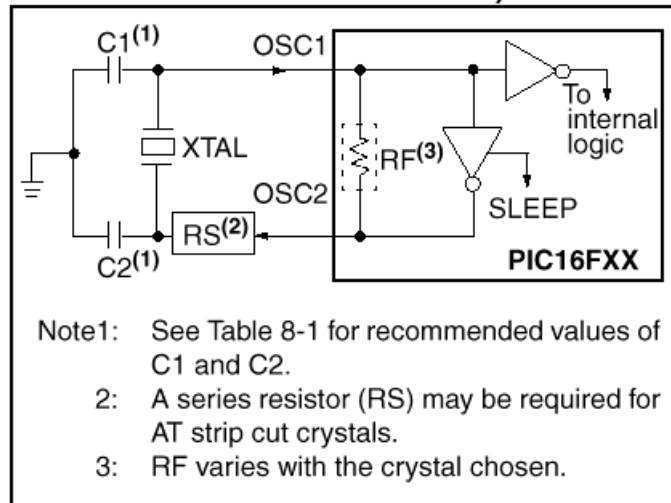


FIGURE 8-4: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

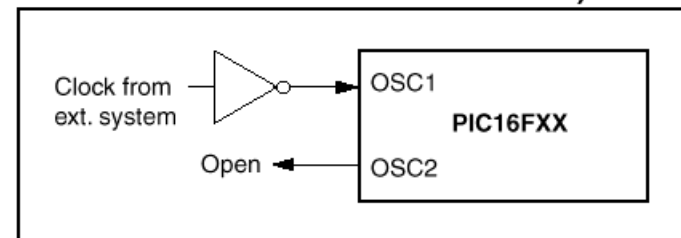
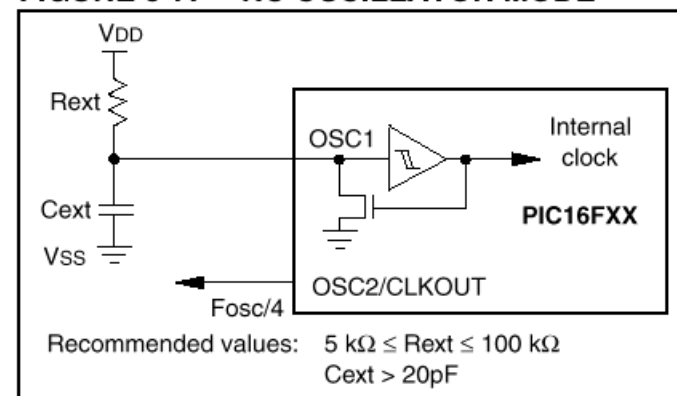


FIGURE 8-7: RC OSCILLATOR MODE



Microcontrolador PIC16F84: Tipos de Reset

Se distinguen cinco clases de RESET:

- Power-on Reset (POR)
- MCLR' reset durante el funcionamiento normal
- MCLR' reset durante SLEEP
- WDT reset durante funcionamiento normal
- WDT Wake-up durante SLEEP

TABLE 8-3 RESET CONDITION FOR PROGRAM COUNTER AND THE STATUS REGISTER

Condition	Program Counter	STATUS Register
Power-on Reset	000h	0001 1xxx
MCLR Reset during normal operation	000h	000u uuuu
MCLR Reset during SLEEP	000h	0001 0uuu
WDT Reset (during normal operation)	000h	0000 1uuu
WDT Wake-up	PC + 1	uuu0 0uuu
Interrupt wake-up from SLEEP	PC + 1 ⁽¹⁾	uuu1 0uuu

Legend: u = unchanged, x = unknown.

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

Microcontroladores PIC

Registros SFR vistos hasta ahora:

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on RESET	Details on page
Bank 0											
00h	INDF	Uses contents of FSR to address Data Memory (not a physical register)								---- --	11
01h	TMR0	8-bit Real-Time Clock/Counter								xxxx xxxx	20
02h	PCL	Low Order 8 bits of the Program Counter (PC)								0000 0000	11
03h	STATUS ⁽²⁾	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	8
04h	FSR	Indirect Data Memory Address Pointer 0								xxxx xxxx	11
05h	PORTA ⁽⁴⁾	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	16
06h	PORTB ⁽⁵⁾	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	18
07h	—	Unimplemented location, read as '0'								—	—
08h	EEDATA	EEPROM Data Register								xxxx xxxx	13,14
09h	EEADR	EEPROM Address Register								xxxx xxxx	13,14
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of the PC ⁽¹⁾				---0 0000	11	
0Bh	INTCON	GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	10
Bank 1											
80h	INDF	Uses Contents of FSR to address Data Memory (not a physical register)								---- --	11
81h	OPTION_REG	RBPV	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	9
82h	PCL	Low order 8 bits of Program Counter (PC)								0000 0000	11
83h	STATUS ⁽²⁾	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	8
84h	FSR	Indirect data memory address pointer 0								xxxx xxxx	11
85h	TRISA	—	—	—	PORTA Data Direction Register				---1 1111	16	
86h	TRISB	PORTB Data Direction Register								1111 1111	18
87h	—	Unimplemented location, read as '0'								—	—
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	13
89h	EECON2	EEPROM Control Register 2 (not a physical register)								---- --	14
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC ⁽¹⁾				---0 0000	11	
0Bh	INTCON	GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	10

Legend: x = unknown, u = unchanged. - = unimplemented, read as '0', q = value depends on condition

Microcontroladores PIC: Interrupciones

Interrupciones en el PIC 16F84:

- Los PICs de la gama media son capaces de manejar 4 fuentes de interrupciones:
 - Externa (pin RB0/INT).
 - Un cambio en los bits RB4 a RB7 del Puerto B.
 - Interrupción del Timer (terminal count).
 - Finalización de la escritura en la memoria EEPROM.
- Existe un único vector de interrupciones en la dirección 0004h.
- El registro INTCON (posición 0Bh, ambos bancos) permite habilitar c/u de las interrupciones (equivalente a las máscaras individuales).
- Este mismo registro contiene flags que sirven para indicar (a la subrutina de servicio) cual fue el origen de la interrupción.
- INTCON además posee un bit de habilitación general (GIE) que afecta a todas las fuentes.

Microcontroladores PIC: Interrupciones

Registro SFR asociado a las interrupciones:

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on RESET	Details on page
Bank 0											
00h	INDF	Uses contents of FSR to address Data Memory (not a physical register)								---- --	11
01h	TMR0	8-bit Real-Time Clock/Counter								xxxx xxxx	20
02h	PCL	Low Order 8 bits of the Program Counter (PC)								0000 0000	11
03h	STATUS ⁽²⁾	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	8
04h	FSR	Indirect Data Memory Address Pointer 0								xxxx xxxx	11
05h	PORTA ⁽⁴⁾	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	16
06h	PORTB ⁽⁵⁾	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	18
07h	—	Unimplemented location, read as '0'								—	—
08h	EEDATA	EEPROM Data Register								xxxx xxxx	13,14
09h	EEADR	EEPROM Address Register								xxxx xxxx	13,14
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of the PC ⁽¹⁾				---0 0000	11	
0Bh	INTCON	GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	10
Bank 1											
80h	INDF	Uses Contents of FSR to address Data Memory (not a physical register)								---- --	11
81h	OPTION_REG	RBPV	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	9
82h	PCL	Low order 8 bits of Program Counter (PC)								0000 0000	11
83h	STATUS ⁽²⁾	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	8
84h	FSR	Indirect data memory address pointer 0								xxxx xxxx	11
85h	TRISA	—	—	—	PORTA Data Direction Register				---1 1111	16	
86h	TRISB	PORTB Data Direction Register								1111 1111	18
87h	—	Unimplemented location, read as '0'								—	—
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	13
89h	EECON2	EEPROM Control Register 2 (not a physical register)								---- --	14
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC ⁽¹⁾				---0 0000	11	
0Bh	INTCON	GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	10

Legend: x = unknown, u = unchanged. - = unimplemented, read as '0', q = value depends on condition

Microcontroladores PIC: Interrupciones

Interrupciones: registro de configuración:

REGISTER 2-3: INTCON REGISTER (ADDRESS 0Bh, 8Bh)

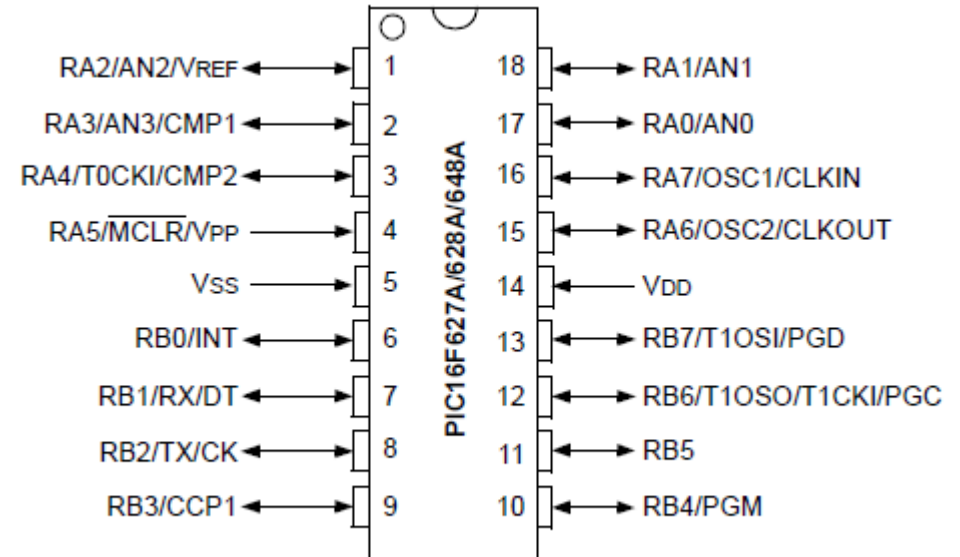
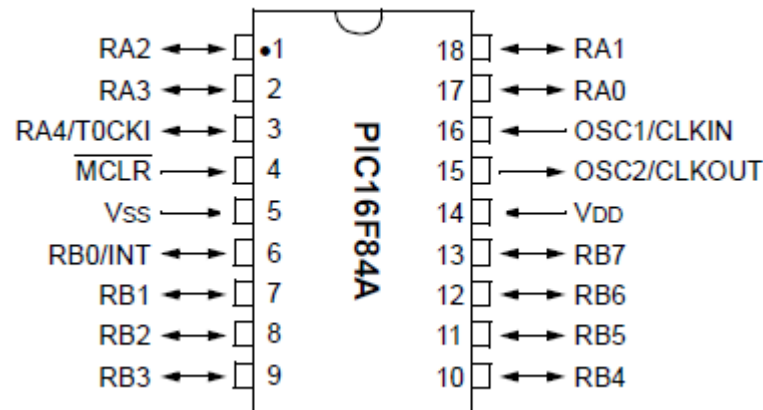
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit 7				bit 0			

bit 7	GIE: Global Interrupt Enable bit 1 = Enables all unmasked interrupts 0 = Disables all interrupts
bit 6	EEIE: EE Write Complete Interrupt Enable bit 1 = Enables the EE Write Complete interrupts 0 = Disables the EE Write Complete interrupt
bit 5	T0IE: TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 interrupt 0 = Disables the TMR0 interrupt
bit 4	INTE: RB0/INT External Interrupt Enable bit 1 = Enables the RB0/INT external interrupt 0 = Disables the RB0/INT external interrupt
bit 3	RBIE: RB Port Change Interrupt Enable bit 1 = Enables the RB port change interrupt 0 = Disables the RB port change interrupt
bit 2	T0IF: TMR0 Overflow Interrupt Flag bit 1 = TMR0 register has overflowed (must be cleared in software) 0 = TMR0 register did not overflow
bit 1	INTF: RB0/INT External Interrupt Flag bit 1 = The RB0/INT external interrupt occurred (must be cleared in software) 0 = The RB0/INT external interrupt did not occur
bit 0	RBIF: RB Port Change Interrupt Flag bit 1 = At least one of the RB7:RB4 pins changed state (must be cleared in software) 0 = None of the RB7:RB4 pins have changed state

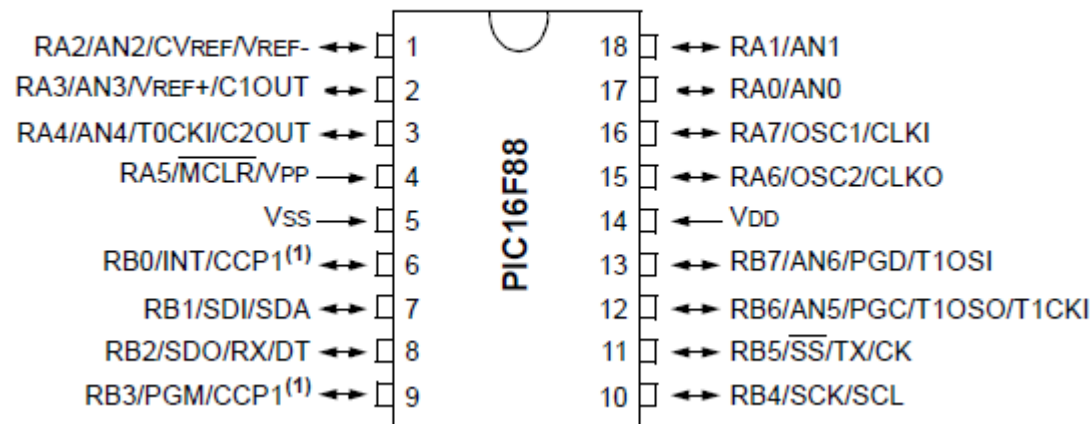
Microcontroladores PIC: 16F628 y 16F88

Versiones más modernas del PIC 16F84: el 16F88 y el 16F628

PDIP, SOIC

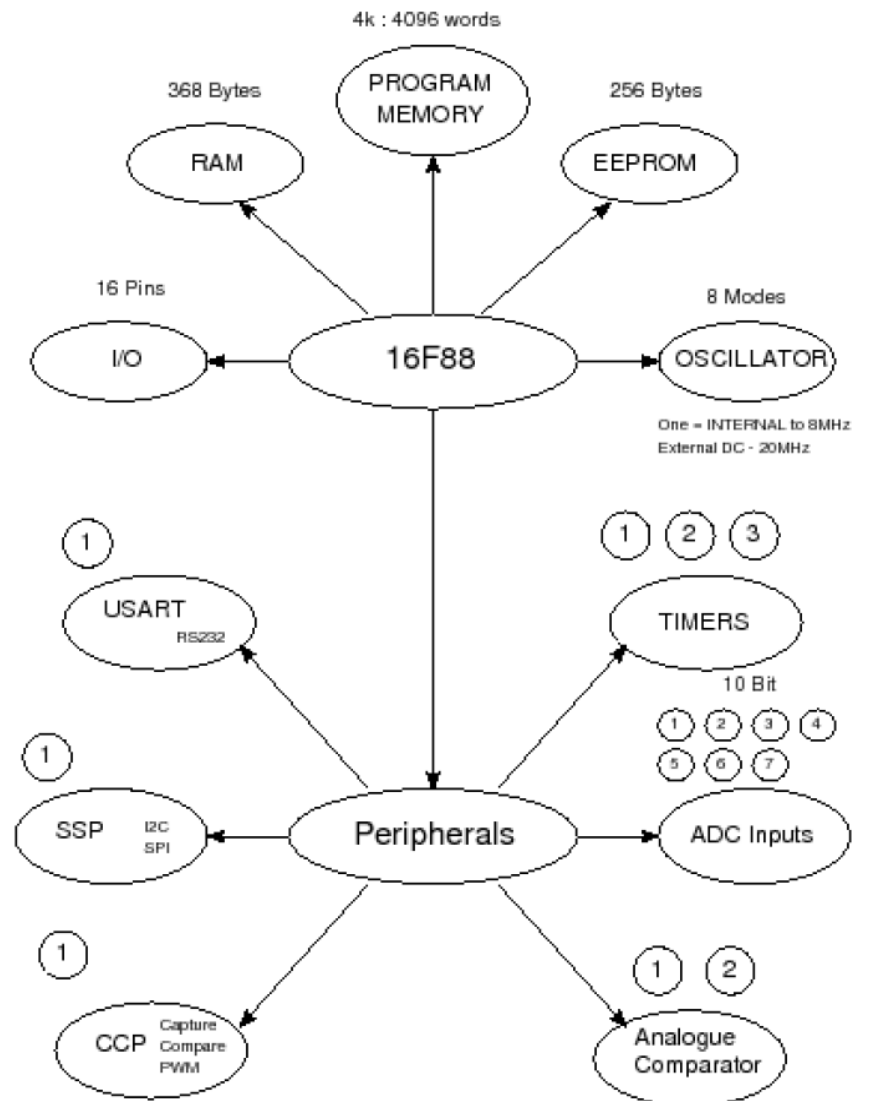
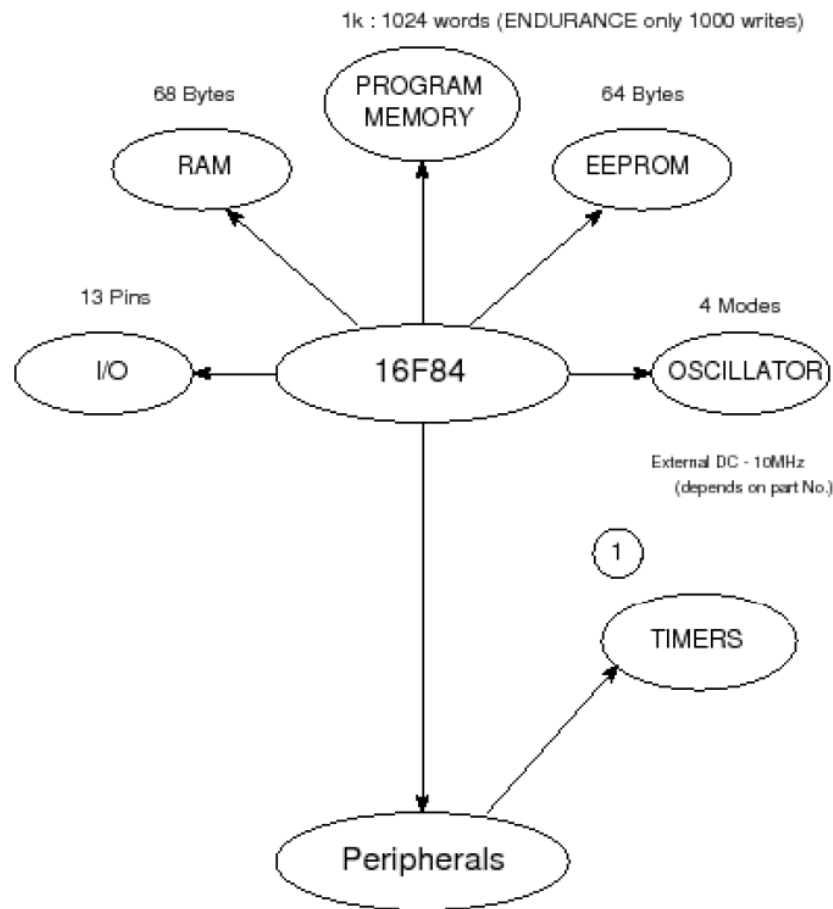


18-Pin PDIP, SOIC



Microcontroladores PIC: 16F628 y 16F88

PIC16F84 vs PIC16F88: Recursos



Microcontroladores PIC: 16F628 y 16F88

Tabla comparativa:

	16F84	16F628	16F88
Memoria de programa (Flash)	1K x 14	2K x 14	4K x 14
Memoria RAM	68	224	368
EEPROM	64	128	256
Pines de I/O	13	16	16
Timers	1 x 8 bits	2 x 8 bits + 1 x 16 bits	2 x 8 bits + 1 x 16 bits
CCP/PWM	-	1	1
ADC	-	-	7 ch, 10 bits
Comparador analógico	-	2	2
Voltaje de operación	2 a 6	2 a 5.5	2 a 5.5
Modos de oscilador	4	6	8
Otras características		- Comunicación USART - Tecnología nanoWatt - Clock interno 4 MHz y 48 KHz LP - LVP	- Comunicaciones SSP, SPI, I²C, USART - Tecnología nanoWatt - Clock interno 8 MHz - LVP, In-Circuit debugging
Precio (Electrónica Mendoza)	?	20	40

Microcontroladores PIC: 16F628 y 16F88

Registro de funciones especiales (SFR)
en el PIC 16F628 (4 bancos):

								File Address
Indirect addr. ⁽¹⁾	00h	Indirect addr. ⁽¹⁾	80h	Indirect addr. ⁽¹⁾	100h	Indirect addr. ⁽¹⁾	180h	
TMR0	01h	OPTION	81h	TMR0	101h	OPTION	181h	
PCL	02h	PCL	82h	PCL	102h	PCL	182h	
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h	
F8R	04h	F8R	84h	F8R	104h	F8R	184h	
PORTA	05h	TRISA	85h		105h		185h	
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h	
	07h		87h		107h		187h	
	08h		88h		108h		188h	
	09h		89h		109h		189h	
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah	
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh	
PIR1	0Ch	PIE1	8Ch		10Ch		18Ch	
	0Dh		8Dh		10Dh		18Dh	
TMR1L	0Eh	PCON	8Eh		10Eh		18Eh	
TMR1H	0Fh		8Fh		10Fh		18Fh	
T1CON	10h		90h					
TMR2	11h		91h					
T2CON	12h	PR2	92h					
	13h		93h					
	14h		94h					
CCPR1L	15h		95h					
CCPR1H	16h		96h					
CCP1CON	17h		97h					
RCSTA	18h	TXSTA	98h					
TXREG	19h	SPBRG	99h					
RCREG	1Ah	EEDATA	9Ah					
	1Bh	EEADR	9Bh					
	1Ch	EECON1	9Ch					
	1Dh	EECON2 ⁽¹⁾	9Dh					
	1Eh		9Eh					
	1Fh	VRCON	9Fh					
CMCON	1Fh							
General Purpose Register 80 Bytes	20h	General Purpose Register 80 Bytes	A0h					
				General Purpose Register 48 Bytes				
	6Fh		EFh					1EFh
	70h		F0h					1F0h
16 Bytes		accesses 70h-7Fh		accesses 70h-7Fh				
	7Fh		FFh					1FFh
Bank 0		Bank 1		Bank 2		Bank 3		